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Microfabrication of Piezoelectric MEMS

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Abstract. In this paper we present an overview of processes for fabrication of piezoelectric thin film devices using PZT ($Pb(Zr_xTi_{1-x})O_3$) in planar structures. These structures are used in cantilever-like and membrane configurations for sensing and actuation. Elaboration of a compatible wet and dry etching sequence for patterning of PZT, electrodes, SiO_2 and silicon substrate is the key issues. The method for compensation of mechanical stresses to obtain flat, multilayer structures is demonstrated. Definition of membrane thickness and release of the structures are obtained by Deep Reactive Ion Etching of silicon (SOI—silicon on insulator substrates) or by surface micromachining. The complete process has been used for fabrication of cantilever arrays, ultrasonic transducers and pressure sensors. Excellent permittivity and transverse piezoelectric coefficient of PZT have been obtained with the final devices. Other examples of applications like: ferroelectric memories, nanopatterning and local growth of PZT are presented as well.

The microfabrication of piezoelectric MEMS was found to be a complex task where all aspects from device design, material properties and microfabrication to assessment of performance are closely interconnected.

Keywords: micromachining, PZT, plasma etching, ultrasonic transducers

Introduction

Piezoelectric thin film are useful in various actuation and sensing devices requiring large output signals, low noise, or high frequency operation (see [1, 2] for a review). An important advantage lies in the fact that a planar structure is able to give excursion and strain detection in the out-of-plane direction, which is very useful for instance in scanning probe techniques [3]. Today, there is a growing interest in the field of micro-electro-mechanical systems (MEMS) for the integration of smart materials with good actuation and/or sensing capabilities. In particular, $Pb(Zr_xTi_{1-x})O_3$ (PZT) and AlN thin films are of primary interest [4].

Piezoelectric MicroElectroMechanical Systems (pMEMS) contain at least two elements: a bulk silicon frame and built on it a piezoelectric deflection element with its electrodes. Micromachining of silicon, which refers to the fashioning of microscopic mechanical parts out of a silicon substrate, has emerged as an extension of IC's fabrication technology [5, 6]. During the last 30 years, it has been successfully employed to produce a variety of mechanical microstructures of a great diversity (beams, diaphragms, grooves, orifices, sealed cavities, pyramids and needles) and has driven the rapid progress of MEMS. However, the silicon substrate represents often only the structural element defining the mechanical properties of the device and, usually, a specific functionality needs to be added. It is the role of functional materials such as piezoelectric thin films to provide a direct transformation between a driving signal or a read-out signal and a sensor or an actuator parameter. The basics of silicon MEMS microfabrication technologies such as photolithography, pattern transfer with dry and wet etching techniques, and common thin films deposition (SiO_2, Si_3N_4, poly-Si, Al, Cr, Ni, Au) have been described extensively in the literature [7]. The microfabrication of piezoelectric MEMS suffers from inadequate micromachining processes and very few references have been published on the subject [8–10]. The integration of piezoelectric thin films like PZT or AlN, and "exotic materials" used as diffusion barrier (TiO_2), electrodes (Pt) or seed layers ($PbTiO_3$) requires new and specific micromachining processes that are not available in standard IC's processing.

The critical tasks, the dry etching of PZT and platinum thin films are, unfortunately, not trivial as the volatility of their reactive by-products is low or very

different for each compound (e.g. the boiling point of: $PbCl_2$: 950°C, PbF_2: 1290°C, $TiCl_4$: 136°C, TiF_4: 284°C, $ZrCl_4$: 334°C, ZrF_4: 600°C [11]). There is thus a need for new patterning processes for PZT and Pt films to afford micro scale resolution at reasonable etching rates and to find a process flow that avoids any degradation of the piezoelectric film.

The aims of this paper are as follow:

- to provide an overview of micromachining tools developed to produce piezoelectric MEMS with microscale features,
- to highlight key issues such as stress compensation, process flow, advanced SOI substrates,
- to demonstrate the fabrication and some properties of PZT/Si microdevices.

Materials and Substrates for pMEMS

Most piezoelectric devices are based on laminated PZT/Si planar structures, which are defined as a flexible supporting silicon structure (5–20 μm thick) coated with a piezoelectric thin film (see Fig. 1). Depending on applications, various geometry and clamping conditions can be considered: from the very simple cantilever to a fully clamped membrane or any partially clamped diaphragms (for instance, membrane fixed to the frame by few bridges). The electromechanical coupling is provided by the transverse piezoelectric coefficient $e_{31,f}$.

To succeed in the microfabrication of such 3D device, a number of important issues have to be addressed:

- the deposition of uniform, high quality PZT and electrode thin films directly on a wafer has to be solved,
- specific micromachining methods and process flow have to be developed,
- the mechanical stress through the structure need to be compensated to avoid any residual bending,
- the thickness of the supporting Si structural membrane should be uniform and the border conditions defined precisely.

Two different techniques have been used to fabricate devices based on planar PZT/Si structures. First, surface micromachining has been mainly employed to make simple accelerometers [12] (ZnO), [13] (PZT). One advantage of this method is that the sacrificial layer (e.g. poly-silicon, PSG) can be used to define precisely the thickness of the supporting structure. However, the etching of the sacrificial layer (PSG) in HF solution often destroys the functional properties of the PZT thin film. Even with a silicon nitride encapsulation, pinholes occurred and the film was damaged. It has been also observed that the roughness of the polysilicon layer disturbs strongly the growth of the PZT film resulting in low piezoelectric coefficients. Finally, the geometries and size of surface micromachined

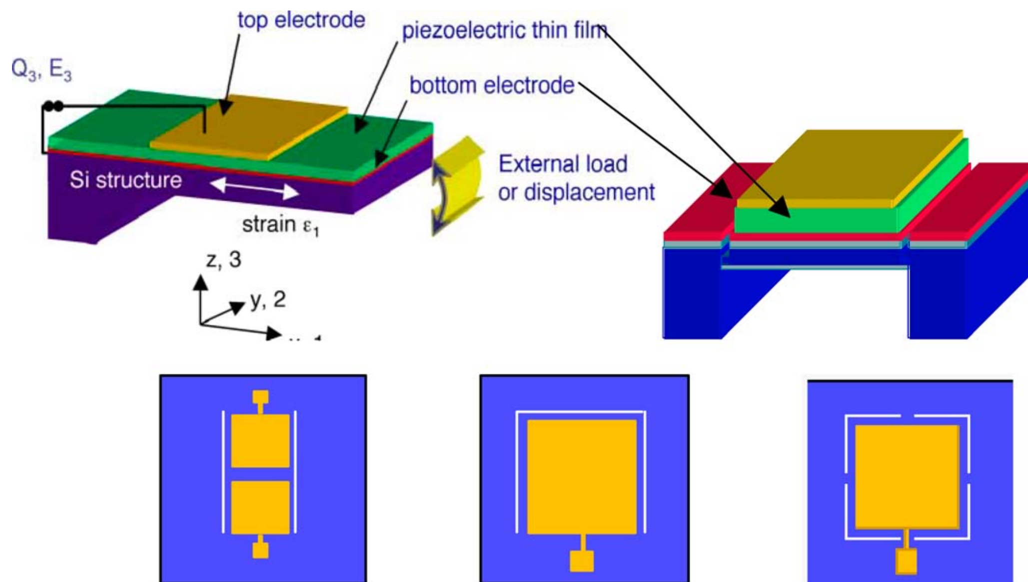


Fig. 1. Laminated PZT/Si deflecting structures used in piezoelectric MEMS: bridge, cantilever and suspended membrane.

piezoelectric devices are limited by the rate of the lateral etching of the sacrificial layer. Beams larger than 50 μm are difficult to release. The second technique is based on classical silicon bulk micromachining. Among reported devices, one can point out micromotors [14, 15] (PZT), [16] (ZnO), accelerometers, [17, 18] (PZT), audio microphone and microspeakers [19] (ZnO), 2-D scanners [20] (PZT), AFM tips [3, 21] (PZT) and ultrasonic transducers [22, 23] (PZT). Here, the limiting factor is a uniformity of the silicon structure obtained with standard wafers. In order to obtain the uniform thickness of a thin Si structure, silicon on insulator wafers (SOI) need to be used. Membranes in thickness range from 0.5 to 50 microns with tolerances better than 1% can be fabricated by DRIE using the buried oxide as etch stop layer. The inconvenience in this type of substrate is the unknown value of the stress in the buried SiO_2.

Films in laminated structures exhibit a mechanical stress (tensile or compressive), which is function of materials and deposition methods. The thin film stress induces bending to the freestanding structure. If the overall residual stress is non zero, a residual bending occurs that can reduce or even destroy the device sensitivity. The stress in piezoelectric PZT thin films depends on composition, texture, thickness and poling [10]. To achieve precise stress compensation, the effect of poling has to be considered as well. Due to the re-orientation of c-domains along the poling field (z-axis), the tensile stress increases further. Table 1 shows that the film stresses of a laminated PZT/Si structure are all tensile except the thermal SiO_2, which is compressive (−300 MPa). Stress compensation is achieved by adjusting the thickness of thermal SiO_2 to about 1000 to 1200 nm, depending on thickness of PZT (Fig. 2).

Processes and Tools for Patterning of pMEMS

Process Flow for the Microfabrication of PZT/Si Planar Structures

Like any IC's classic process flow, the microfabrication of planar PZT/Si deflecting structure is based on several iterations of film deposition—photolithography—etching [7]. Figure 3 shows the generic process flow for the microfabrication of planar PZT/Si suspended membrane structures. Starting with doubleside polished and oxidized silicon based substrate (Si wafer, SOI, polySi on SiO_2/Si), an adhesion layer (e.g. Ti/TiO_2), a bottom electrode (e.g. Pt) and a seed layer (e.g. $PbTiO_3$, TiO_2) are deposited by PVD sputtering [24, 25]. On top of seed layer, the piezoelectric thin film is deposited by sol-gel CSD [10] or by sputtering [26]. Top electrode is deposited and patterned either by lift-off (Au/Cr) or by plasma dry etching (Pt, Cr, Al). To give access to the bottom electrode, vias are opened through the PZT film by wet or dry etching. The frontside shape of the structure (the grooves or gap surrounding the membrane) is then patterned through the PZT/Pt/SiO_2 stack and through Si defining the depth of grooves. Bulk silicon micromachining from the wafer's backside is then performed to define the thickness of the structure (usually between 5 and 20 μm). The process is either dry (deep silicon etching in a plasma reactor) or wet in KOH solution (see [6] for review). The definition of precise and uniform silicon thickness (for example: 5 to 20 ± 0.2 μm thick silicon cantilever out of a 390 μm thick wafer) is of primary importance as the device sensitivity is usually a function of 1/thickness.[2] In order to increase the precision of membrane thickness definition several solutions are proposed:

Table 1. Typical materials used in PZT/Si deflecting structures.

Materials	Growth methods	Thickness	Typical stress (MPa)	Patterning methods
Silicon wafer/SOI	Czochralski/bonding and polishing	390 micron; 1 to 50 μm of device Si on burried SiO_2		DRIE; wet etching (KOH, TMAH)
Thermal SiO_2	Wet oxidation	Max. 2000 nm	-300 ± 5	ICP plasma etching; wet etching (BHF)
Si_3N_4	LPCVD	Max. 200 nm	0 to + 700	ICP plasma etching
Pt bottom electrode	PVD sputtering	100 to 300 nm	+550	ICP plasma etching
PZT 53/47 {100}	Sputtering or sol-gel	500 to 4000 nm	+110 (*unpoled*) +180 (*poled*)	ECR/RF plasma etching; wet etching (HCl/HF)
Au/Cr top electrode	PVD evaporation	100 nm/10 nm	+280	Lift-off

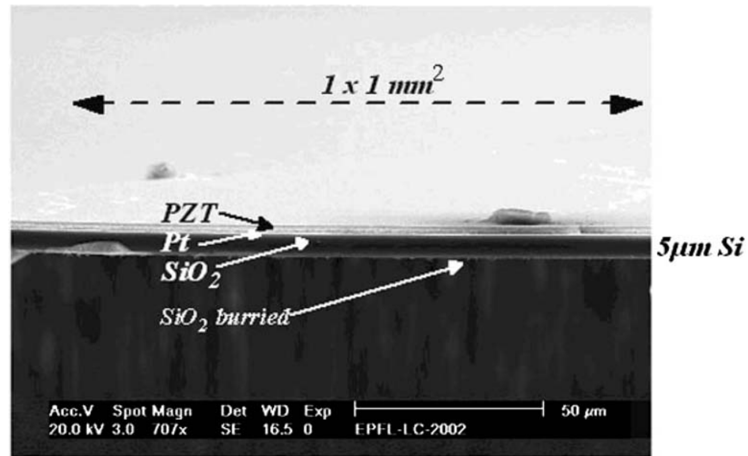


Fig. 2. SEM cross-section of flat PZT/Pt/SiO_2/Si square membrane (7 micron thick and 1 × 1 mm^2 large).

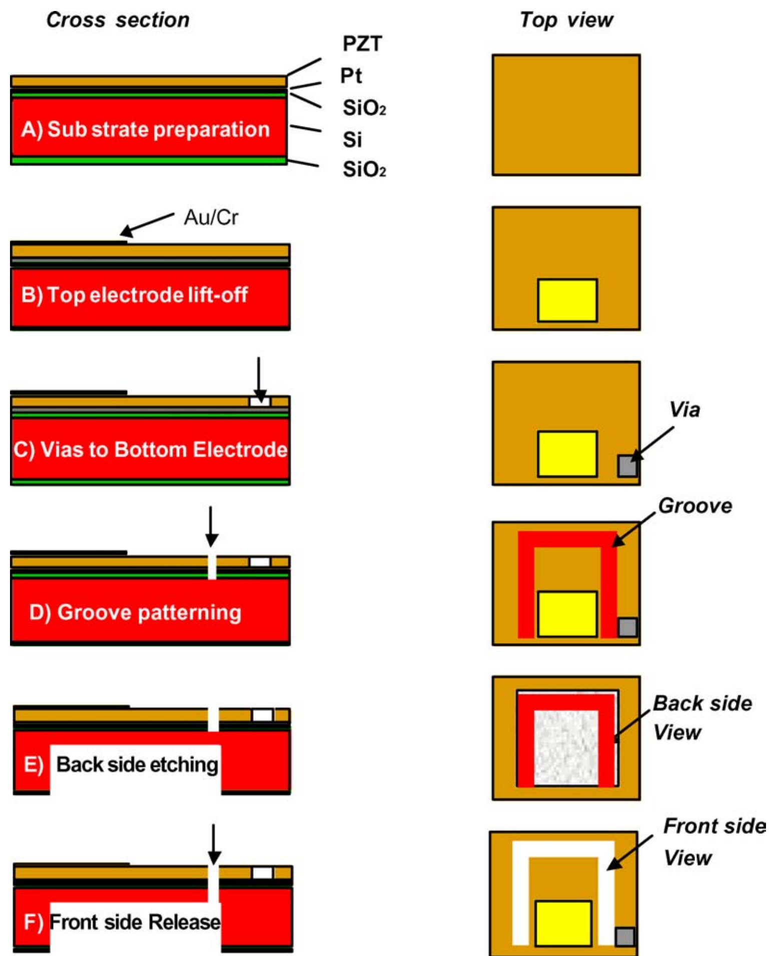


Fig. 3. Generic process flow for the microfabrication of PZT/Si cantilever (cross section and top view).

- accurate etching time measurement supposing constant process conditions,
- etch-stop obtained on n-doped epi-layer [27],
- Silicon-On-Insulator (SOI) used as substrate [23].

The micromachining steps of this process flow use many individual deposition and patterning processes. Details on general issues such as photolithography or silicon thermal oxidation can be found in [7] or in the process book of the Center of Microtechnology (CMI) at EPFL [28]. However, some of the processes are specific for microfabrication of piezoelectric MEMS and are described below.

Basics of Patterning

Dry etching using reactive plasma has spread widely throughout the VLSI processing field because of its ability to fabricate fine-line semiconductor devices. However, the resolution of conventional Reactive Ion Etching (RIE) when decreasing the size of patterns is limited, because the operation pressure of RIE is too high to etch these patterns anisotropically. Moreover it is difficult to obtain a high etch rate because the plasma density of conventional RIE is limited. In case of piezoelectric MEMS the additional difficulty is related to the patterning of noble metals or refractory oxides, both exhibiting very low volatility. To overcome at least partially limitations of patterning such structures, a new process using high density plasma with low ion energy (to avoid damage of the piezoelectric layer and of the photoresist) and operating at lower pressure (lower backscattering, no fencing) is required. The most popular are actually inductively coupled plasma (ICP) sources (see [29] for review). However, other type of reactors like Helicon Wave Plasma (HWP), planar Electron Cyclotron Resonance (ECR) or Multifrequency Reactors (ECR/RF, RF/HF) have been extensively studied for laboratory and industrial applications [30–32]. Recently the possibility of high anisotropic etching of submicron Ir/PZT/Ir ferroelectric capacitors by using a Dual Frequency High Density reactor operating at 380°C has been reported [33, 34].

PZT piezoelectric MEMS microfabrication requires many different thin film patterning processes as well as silicon bulk micromachining. In following sections, selected topics that are specific to the microfabrication of piezoelectric devices will be presented:

- Top electrodes patterning
- Wet and dry methods for patterning of thin PZT films,
- Dry etching of bottom electrodes (platinum, RuO_2, iridium)
- Silicon bulk and surface micromachining.

Patterning of Top Electrodes

To collect the electrical charges on the PZT film different types of electrodes need to be deposited and patterned (Au/Cr, Pt).

Compared to platinum, Au/Cr top electrode has two advantages:

- the patterning of Au/Cr top electrodes does not require plasma methods, as lift-off process is very versatile and offers sufficient resolution (micron scale) for MEMS applications,
- Au/Cr top electrodes do not need post-deposition annealing.

The top electrode is deposited by Joule effect (Au) and e-beam source (Cr) in evaporator and patterned by lift-off using a negative photoresist. Figure 4 illustrates the Au/Cr top electrode obtained by lift-off on $50 \times 1000\ \mu$m cantilever. The lateral resolution is only limited by the resolution of the mask.

Platinum top electrode is obtained in three steps:

- PVD deposition of 100 nm Pt at room temperature,
- High temperature annealing to increase the adhesion, to restore the interface Pt/PZT and to recrystallize Pt

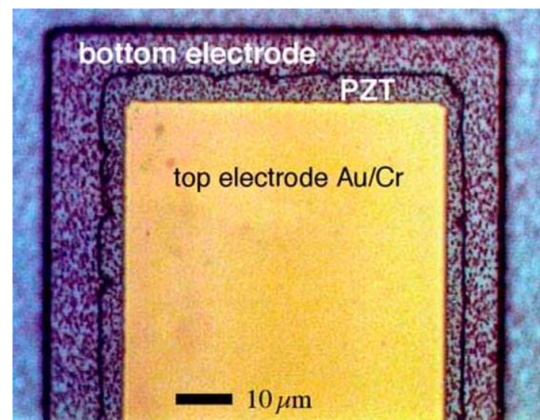


Fig. 4. Optical image of top view of the tip of a $100 \times 500\ \mu m^2$ PZT/Si cantilever.

- Photolithography and dry etching to shape the top electrode (effective size of device).

With PVD deposited platinum, the PZT surface is damaged by the ions bombardment as well during deposition and etching. Thermal annealing is then required to restore the interface [35]. This method enable the patterning of submicron precision of device forms.

Wet Etching of PZT Thin Films

The wet patterning of PZT thin films is a critical point in piezoelectric MEMS microfabrication. Despite the lack of etch control and photoresist undercut, the wet etching of PZT films remains a very versatile, fast and cheap method to open large areas (>50 × 50 μm^2) like vias, with rather poor lateral resolution control. Because of high concentrations of hydrofluoric acid (HF), most of etch recipes are not selective to SiO_2 and to the TiO_2 (adhesion layer of the platinum bottom electrode). Delaminating of the structure can thus occur. In term of etching rate, HCl solutions are very effective and selective etchants [36]. In our works, the standard solution of 30 ml of concentrated HCl (37%), 70 ml of water and 0.2 ml of HF has been used. At 56°C, the etching rate is about 50–100 nm/s. Figure 4 shows the top view of a 500 × 100 μm^2 microcantilever where the 1 μm PZT film has been patterned by wet etching. Underetching and profile irregularities as large as 5–10 μm can be observed which give a masks design rule (geometry tolerance) of about 10 times the PZT thickness (Fig. 5). Under these conditions wet etching of narrow patterns (e.g. grooves of width 3–10 μm, capacitors below 25 μm^2) is thus impossible and dry etching techniques should be employed.

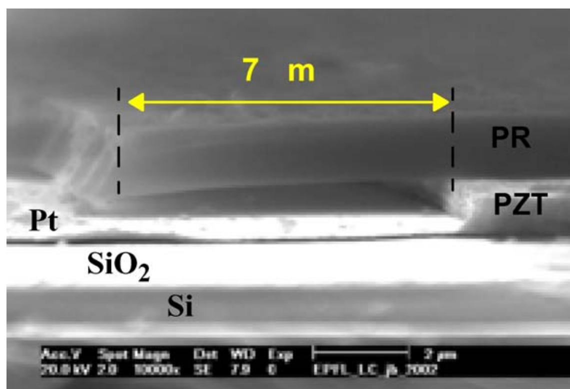


Fig. 5. SEM image cross-section of photoresist/PZT after wet etching (lateral underetch is 7 μm for 1 μm thick PZT layer).

Dry Etching of PZT Thin Films

As the size of MEMS critical features shrank to several microns (<10 μm), the dry etching of PZT becomes mandatory to obtain a high degree of anisotropy, smoothness and preserved shape of profiles. The principal requirements for a dry etching process of PZT films are:

- Sufficient selectivity to the photoresist (higher than 0.5) and with respect to the bottom electrode (Pt),
- High anisotropy to define precise micron-scale geometries (e.g. grooves, capacitors),
- High etching rate,
- No damage to the piezoelectric films and no patterning residue.

The dry etching of PZT films is not obvious as there is no common halogenous gas that forms volatile compounds with all three elements (Pb, Zr, Ti) to guarantee the residue free removal of film. The volatility of the reactive etch by-products of Pb, Zr and Ti is variable and limited [37] and energetic ion bombardment is often required to obtain the uniform removal of PZT layer. First developed processes used pure argon ion milling or Reactive Ion Etching (RIE) in simple parallel plate or inductively coupled plasma (ICP) reactor. Zeto [38] demonstrated etch rates up to 100–250 nm/min with argon ion milling. However, sloped walls (35–70°), low selectivity to the platinum bottom electrode and photoresist mask as well as material redeposition on the sidewalls were the limiting factors. To overcome these drawbacks, Reactive Ion Etching (RIE) with halogenous gases should be employed. Chlorinated plasmas were generally employed because of the low melting point of metal chlorides with respect to the equivalent metal fluorides (e.g. $PbCl_3$, PbF_4). However, fluorine ion bombardment (CF_4, SF_6, C_2F_6) was shown to be more selective with respect to the platinum electrodes.

Etch rate of PZT has been increased up to 100 nm/min with monochlorotetrafluoroethane (HC_2ClF_4) as etch gas and 500 W RF power in a standard parallel plate reactor [38], but in this case, the stability of the photoresist was the limiting factor. For films thicker than 250 nm, the RF power has to be dramatically reduced down to 150 W to keep the photoresist mask removable. At such power level, the etching rate is only 13 nm/min. This example is representative

Table 2. Process characteristics for etching of PZT and Pt with ECR/RF ion gun [30, 45].

	PZT etch process	Platinum etch process
Gases	40% CCl_4/40% CF_4/20% Ar	85 % CCl_4/15 % Ar
Pressure	10 mPa	5 mPa
RF bias	60 W (max 0.75 W/cm^2)	50 W (max 0.65 W/cm^2)
Etch rate	max 70 nm/min	max 45 nm/min
Selectivity	0.5 to photoresist, 1.5 to Pt	0.75 to photoresist, 2.5 to PZT
Mask	Shipley 1818, 2.3 μm, hard bake at 150°C, 30 min, air oven	Shipley 1805, 1.5 μm, hard bake at 150°C, 30 min, air oven

of the problems occurring in RIE of PZT films. It is very difficult to find a trade-off between a reasonable PZT etch rate, photoresist dimensional stability and removability. Other studies gives similar results in term of etching rates (10 to 40 nm/min) in HC_2ClF_4 [39], in C_2F_6/Cl_2 [40] or in CF_4/Cl_2 [41] gases recently, Chung et al. [42] reported the etching process of PZT using ICP reactor and HBr/Ar gas mixture. An etch rate of 90 nm/min and a steep etch profile of 70° has been achieved.

Reactive Ion Beam Etching (RIBE) in a dual frequency ECR/RF reactor [43–45] allows much lower working pressure than the RIE/ICP process (1 to 10 mPa compared to 1–10 Pa). The risk of material redeposition is reduced and the verticality of the sidewalls is improved thanks to the directionality of the bombarding ion beam. The bombardment of a reactive ion beam with gases such as SF_6, CF_4 or CCl_4 is very favorable to reduce the level of energy needed for the etching process and thus to obtain better trade-off between photoresist stability and etching rate.

The homemade reactor we used was based on a commercial ECR ion gun [44] as illustrate in Fig. 6. The capacitive coupling of the substrate holder to a 13.56 MHz RF power supply contributes to the acceleration of the ions bombarding the substrate (negative bias voltage).

For RIBE of PZT films, a process with low ion energy ions and low operating pressure (see Table 2) has been developed. Best results were obtained by mixing both chlorine and fluorine gases and light Ar ion bombardment [45]. Photoresist stability was improved by hard baking at 150°C in air and by keeping the moderate ion bombardment (<0.75 W/cm^2) during process. Dense, up to 1 μm thick PZT films have been etched with anisotropy close to 90°, without residues and without degradation of PZT properties.

Figure 7 shows PZT thin films etched with ECR/RF RIBE using low working pressure (0.01 Pa) and moderate RF bias (below 0.75 W/cm^2). In this case, vertical profiles and micronscale patterns have been obtained. As the working pressure is increased to 0.5 Pa and the RF bias to 120 W, the anisotropy of patterns is low and due to the high energetic ion bombardment the photoresist is hardly damaged (Fig. 8).

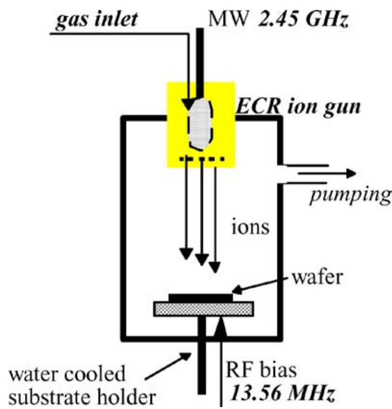


Fig. 6. Schema of dual frequency ECR/RF RIBE reactor [44, 45].

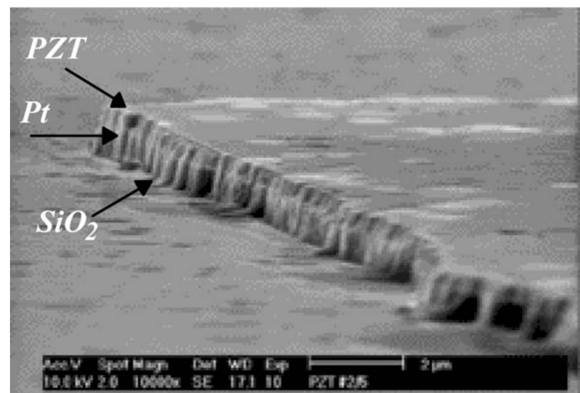


Fig. 7. SEM side view image of patterned PZT thin film, working pressure = 0.01 Pa, 60 W RF bias, optimized etching chemistry. Photoresist mask removed [45].

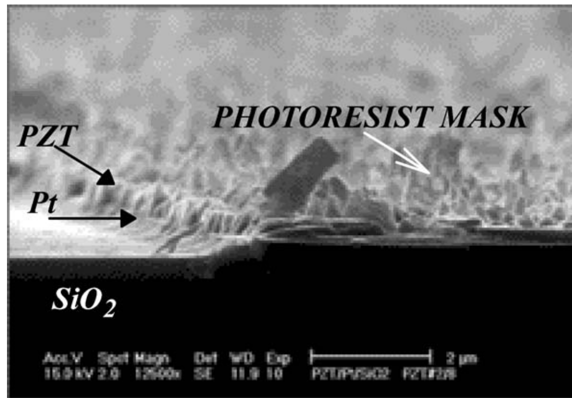


Fig. 8. SEM side view image of patterned PZT thin film, working pressure = 0.5 Pa, 120 W RF bias, optimized etching chemistry.

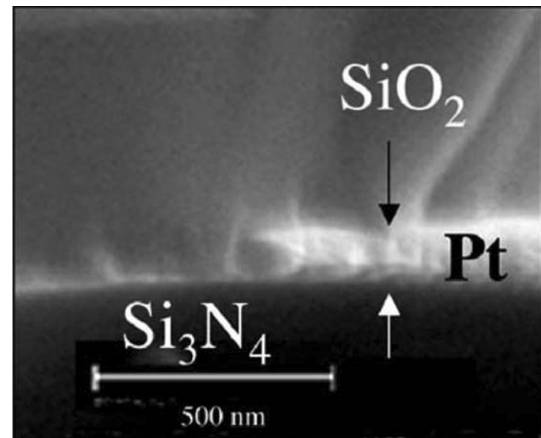


Fig. 9. SEM image cross-section of dry etched Pt on Si_3N_4 membrane.

Dry Etching of Bottom Electrodes

Platinum. Ferroelectric thin films for MEMS or memory applications require noble metal (platinum, iridium) or conductive metal oxide (RuO_2, IrO_2) electrodes. Due to their chemical inertness, the patterning of these materials is a difficult task. The platinum thin films can be patterned by wet etching; aqua regia [46] or electrochemical wet etching in concentrated HCl [47] are the most known methods. However, these recipes do not work with very thin structures (below 10 μm), are very sensitive to the platinum surface contamination, are often subject to underetching of the adhesion layer and, the selectivity to PZT is very low.

For piezoelectric MEMS, HDP dry etching techniques have to be chosen. There is only a small number of volatile compounds that can be formed with platinum (e.g. $PtCl_3$ decomposes at 370°C in Cl_2, PtI_2 decomposes at 270°C). In fact, the etching mechanisms are much more physical (ion bombardment) than chemical (formation of volatile reaction products). Most of recent developed methods have used RIE/ICP (Reactive Ion Etching with Inductive Coupled Plasma reactors), simple Ar ion milling or ECR/RIBE. In all cases [48, 49] several common limitations have been observed:

- Selectivity problems with photoresist
- Hard masks (TiN, SiO_2) masks are not common to use in presence of PZT,
- Metal residues on the sidewalls lead to fencing,
- Poor patterns anisotropy with ion milling
- Due to the strong ion bombardment photoresist mask gets harder and its after stripping the organic residues remain.

In our studies, chlorine based RIBE process with dual-frequency ECR/RF plasma [30, 31] (see Table 2). Figure 9 shows a SEM image cross-section of the edge of 100 nm thick Pt film deposited on Si_3N_4/SiO_2 membrane. The anisotropy of the pattern is close to 90° and the selectivity to Si_3N_4 is excellent (no overetch into Si_3N_4).

With a RIE/ICP reactor from STS, best results have been obtained with Cl_2 flow rate of 20 sccm, Ar flow rate of 70 sccm, working pressure of 1 Pa, RF plasma power of 800 W and RF substrate bias power of 150 W. The etching rate was lower (32 nm/min) than the one obtained by RIBE and the selectivity was 0.35 and 0.5 with respect to standard photoresist (Shipley 1805) and SiO_2 respectively. Figure 10 shows the profile of Pt/SiO_2 after ICP etching at 1 Pa. The curved shape

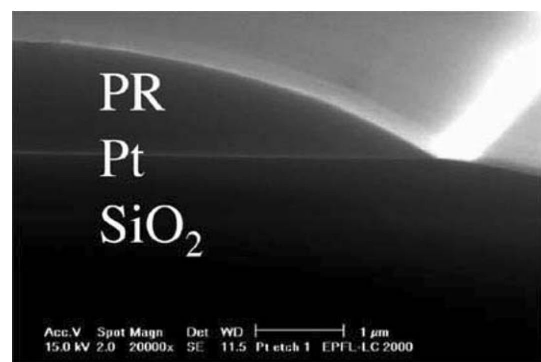


Fig. 10. SEM image cross-section of ICP dry etched Pt film.

of the photoresist and the thin film is typical of highly physical dry etching process. However, any redeposition of the metal on the mask sidewalls has not been observed. Both processes for Pt etching (RIBE/ECR and RIE/ICP) offer a good selectivity to PZT (>2) and have been successfully applied for the patterning of platinum top electrodes. The photoresist mask is striped in Shipley Microposit Remover 1165 at 70°C followed by low power microwave plasma aching in oxygen [10].

Iridium. The patterning of Ir electrode is mostly related to fabrication of FeRAMs capacitors [50, 51]. RIE/ICP etching of iridium has been related by several groups [52–55]. Chung et al. has used a hard mask (TiO_2) [52] or photoresist mask [53] testing chlorine, bromide and fluorine chemistries ($Cl_2/O_2/Ar$; $HBr/O_2/Ar$; $C_2F_6/O_2/Ar$, $C_2F_6/Cl_2/Ar$). Etch rates 40 to 60 nm/min have been obtained with chlorine. Clean profiles with Cl_2 and HBr when using a hard mask and with fluorine when using the photoresist were observed. Residue-free patterns, 50° sidewalls with fluorine-chlorine gases and Ar addition have been finally obtained. Xu et al. [54] has established the process for etching of Ir electrical contacts. By using XeF_2, in presence of Si source a good selectivity to IrO_2 and Pt has been achieved and Ir/PZT/Ir capacitors remained non-affected. Chiang et al. [55] has employed the $Ar/O_2/BCl_3$ gas mixture and TiN hard mask. The selectivity Ir/TiN up to 10, the Ir etch rate up to 66 nm/min (60%Ar/20%O_2/20%BCl_3, 1500 W bias), fence free patterns and vertical (>70°) sidewalls were observed. Patterning of Ir/IrO_2/PZT submicron, ferroelectric stack has been demonstrated and commercialized by Tegal [33]. Using the double frequency High Density Plasma reactor operating at 380°C the etching rate of Ir up to 100 nm/min with the sidewall profile better the 85° have been presented.

Etching of Ir/IrO_2 stack for FeRAM applications was done with ECR/RF Ion Gun [10]. The 100 nm thick iridium bottom electrode was etched in 80%CCl_4/20%Ar mixture. Increasing of CCl_4 rate flow induces some enhancement of etching, however, a saturation of removal rate occurs when limited by formation of $IrCl_4$ product (Fig. 11). Despite, the etch rate of Ir can be stimulated by RF substrate bombardment, the maximum etch rate 15 to 20 nm/min was obtained. Micronscale resolution patterns without any impact on properties of ferroelectric capacitor or transistors have been realized (Fig. 12).

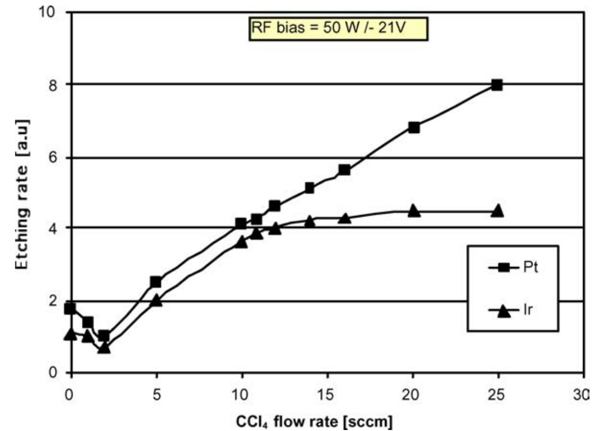


Fig. 11. Comparison of etching rates of Pt and Ir as function of CCl_4 percentage in ECR/RF RIBE [10].

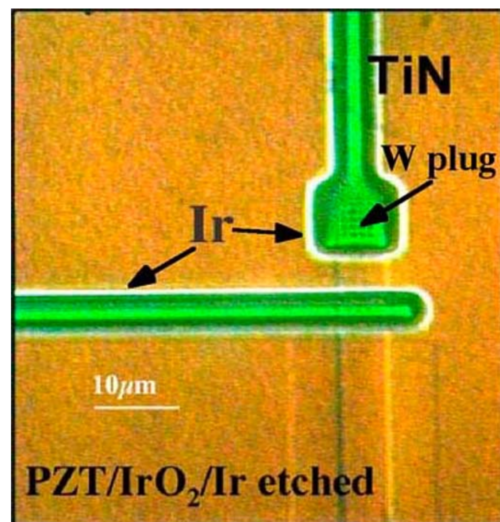
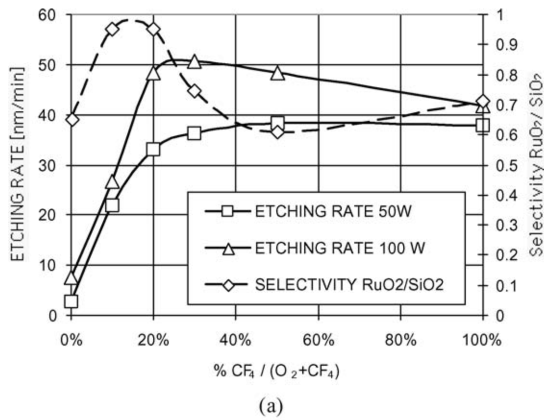


Fig. 12. Top view of PZT/IrO_2/Ir stack etched with ECR/RF RIBE.

Ruthenium oxide. For RuO_2 it has been reported that the etching in oxygen plasma is effectuated by the formation of volatile RuO_4 [56] and this process can be catalyzed by small addition of Cl- or F-based gas to O_2 plasma [57]. Most of these experiments were carried out in RIE/ICP systems where independent control of the energy and flux of the reaction species is not easy. Moreover, the working pressure range is usually about several pascals reducing the anisotropy and creating the polymer like residues. Unlike Lee [56], a very low etch rate with Cl was obtained even if O_2 was added. Only fluorine-containing gases or gas mixtures provide



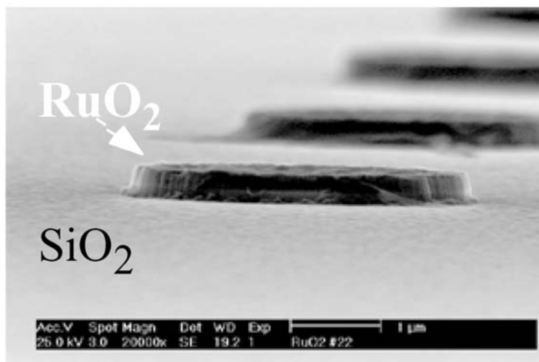
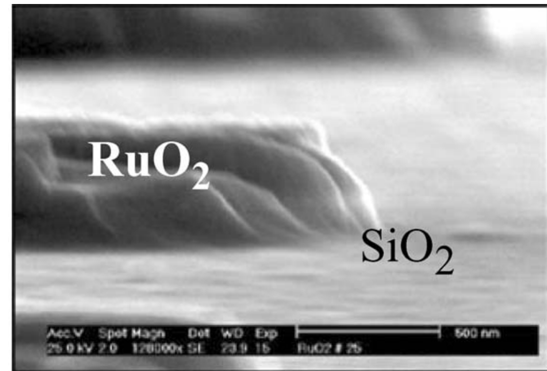


Fig. 13. Etching of RuO_2: (a) effect of CF_4 concentration on etching rate of RuO_2 and the selectivity SiO_2/RuO_2, (b) 3 × 3 micron^2 patterns obtained with ECR/RF RIBE [31].



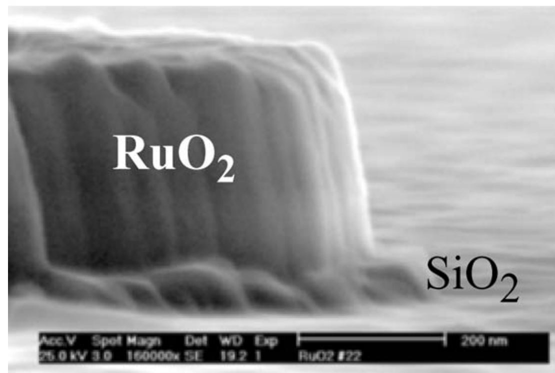


Fig. 14. Profiles of RuO_2 patterns obtained with (a) SF_6/O_2, (b) CF_4/O_2 mixture.

reasonable etch rates [31]. As suggested by Desu [57] a small addition of fluorine gas to oxygen increases significantly the etching rate. When the CF_4/O_2 is used, the addition of 25% of CF_4 induces the increase of etching rate from 10 to 50 nm/min at 100 W RF bias and from 7 to 35 nm/min at 50 W RF bias (Fig. 13(a)). An interesting correlation with the selectivity to SiO_2 occurs—for low quantity of CF_4 the selectivity is poor because of low etching rate of RuO_2. On the other hand, the high (above 50%) proportion of CF_4 induces higher etch rate of SiO_2 which reduces the selectivity again. Finally, an optimal proportion of 20% CF_4/O_2 allows to achieve both high etching rate and good selectivity to SiO_2 underlayer. As shown in Fig. 13(b), the $3 \times 3\ \mu m^2$ patterns through 300 nm thick RuO_2 can be obtained with anisotropy higher than 80°. Smooth SiO_2 substrate surface is visible and no polymer-like residue due to decomposition of CF_4 [56] was observed; this fact is due principally to a low working pressure (typically 10 mPa) in ECR/RF system. Figure 14 shows the difference in etched profiles of RuO_2 when using (a) SF_6/O_2 and (b) CF_4/O_2 mixture; for the same process conditions the etch rates were similar, but etching in SF_6/O_2 results in lower anisotropy of patterns and lower selectivity to SiO_2.

Silicon Bulk Micromachining

To produce thin silicon supporting structures like beams or diaphragms, bulk silicon has to be etched in a uniform way, down to the desired thickness (usually thinner than 20 μm). As the sensitivity of a sensor based on a cantilever is proportional to 1/(silicon thickness)^2, precise control of the silicon thickness has a direct influence on the production of uniform and homogenous devices. To control accurately the thickness of the silicon

structures, many wet-etching methods (KOH, TMAH) using an etch-stop on a very well defined n-doped epi [27] or highly p-implanted silicon layers have been developed [6]. However, these methods suffer from difficult and complicated process implementation and stress non-uniformity. Despite a very low running cost, bulk silicon micromachining in KOH has important drawbacks:

- the shapes of the structures are restricted by the etching anisotropy (for example, V-grooves of 10 μm wide cannot achieve a depth larger than 7 μm due to the lower etching rate of the (111) planes),
- the etch rate of silicon in KOH depends not only on solution concentration and temperature, but also on impurity presence in Si wafer,
- the KOH is very aggressive against the PZT and its electrodes,
- the uniformity is limited to about $\pm$10–15 μm after etching 380 μm of silicon.

The dry and anisotropic plasma etching process offers much more flexibility in term of design and is the solution of choice to define accurately small structure like very narrow gaps, grooves and even large surface in case of membrane patterning. The most commonly used process for deep silicon etching is the so-called “Bosch process” invented by Lärmer and Schilp [58]. By sequentially alternating etching steps (with SF_6 chemistry) and passivation steps (polymerization of the sidewall with C_4F_8), a deep anisotropic etching can be obtained on feature sizes ranging from submicron to several millimeters [59]. High etching rate of 7–10 μm/min enables a rapid fabrication of deep trenches and membranes. Figure 15(a) shows a SEM cross-section of a 10 $\times$ 50 μm trench. Vertical sidewalls with aspect ratio of more than 1:15 have been obtained when using Pt bottom electrode as a hard mask (Fig. 15(b)) [10]. However, defining precise and uniform membrane thickness all over a wafer by deep silicon etching is a difficult task. It can be observed in Fig. 15(c)) that the bottom of the etched cavity is neither flat nor perpendicular to the sidewalls. This phenomenon can be explained by the ion scattering effect at the

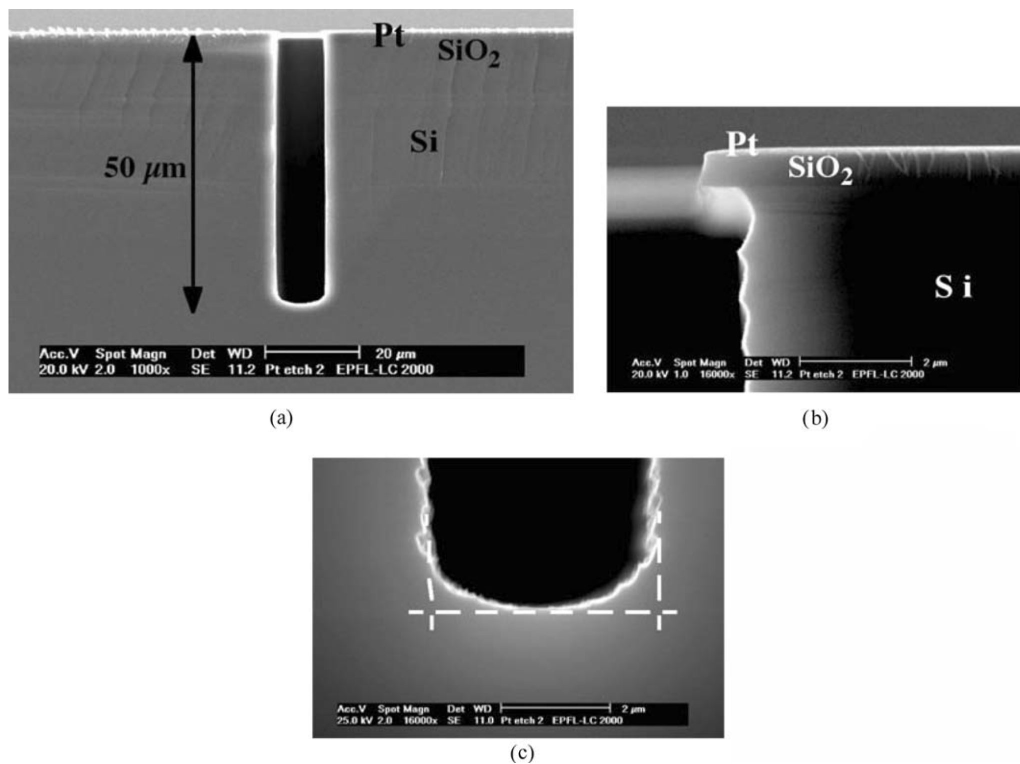


Fig. 15. SEM images cross section of 10 $\times$ 50 μm (AR = 15) groove etched by optimized Bosch process into silicon, and details of 3 μm large slit. Pt hard mask has been used [10].

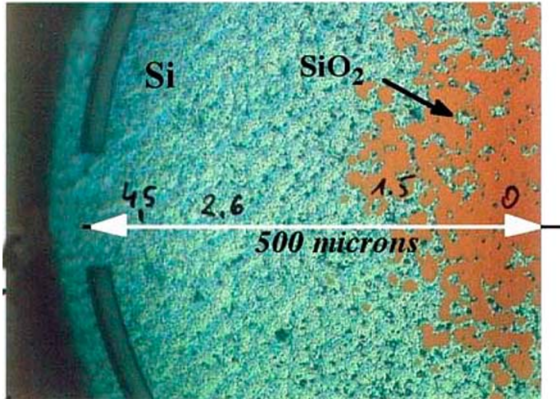


Fig. 16. Non uniformity of Si thickness at the bottom of 1 mm^2 large Silicon membrane.

sidewalls and creates a non-uniformity of the membrane thickness (thicker near the clamping point) that can amount to several microns. Figure 16 shows the non uniformity of Si thickness at the bottom of 1 mm large membrane [9]. The Si thickness increases from 10 μm at the membrane outskirts to zero in the membrane center, where the underlying SiO_2 layer is clearly visible. This difficulty in removing of Si near the clamping point limits the minimum thickness of short cantilevers, as shown in Fig. 17. For presented here 50 × 20 μm cantilever the nominal thickness of 10 μm could not be achieved. Furthermore, on the wafer level, a depth uniformity of about 3% (± 5 μm in 380 μm deep cavities or 10 μm thick membranes) is typical even with well-tuned process. This leads to the quite large dispersity of membrane properties and performances across the same wafer. To overcome, at least partially, these

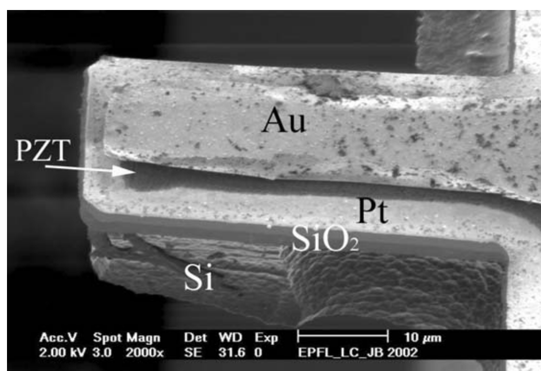


Fig. 17. SEM view of 50 × 20 μm^2 cantilever. The nominal thickness was 10 micron.

limitations, an etch-stop on a buried silicon oxide layer may offer an interesting solution.

The combination of short time isotropic and anisotropic plasma etching of Si using photoresist/SiO_2 mask is demonstrated in Fig. 18. These methods are basically used for shapening of tips and arrays of microneedles.

Integration of PZT Films on SOI and Polysilicon Substrates

Silicon-on-Insulator (SOI) or poly-SOI substrates can be used to improve the uniformity of the structure thickness on the wafer scale. These two substrates use mono- or polycrystalline silicon layer deposited on insulating and amorphous SiO_2 thin film; the latter acts as an etch-stop during the bulk silicon micromachining (DRIE) or can be used as sacrificial layer for surface micromachining.

In SOI wafers, the device silicon thickness (top silicon layer) is usually ranging from 0.2 μm to several hundreds of microns and the deposition of PZT films and process flow do not differ from processing on classical silicon substrates. Figure 19 illustrates example of so fabricated PZT/SOI 5 μm thick membrane surrounded by the 20 μm large and 4 μm deep grooves [9]. When using thick polysilicon layer (up to 4 microns thick), additional processing steps are required as the roughness of the film is high (≈300 nm RMS) after deposition by LPCVD. This roughness introduces random crystallization of PZT. To recover the surface state of polished silicon wafer, Chemical-Mechanical-Polishing (CMP) [60] of poly-silicon has been used and 200 nm SiO_2 passivation layer have been then deposited by PVD. Figure 20 shows SEM image of the cross section of 1 μm PZT 53/47 {100}-textured deposited on $PbTiO_3$/Pt/TiO_2/SiO_2/poly-Si/SiO_2/Si substrate. No cracks and no delamination have been observed showing the excellent stability of the PVD SiO_2/poly-silicon structure during the processing of PZT and excellent functional properties have been also obtained: $e_{31,f} = -11$ C/m^2, $\varepsilon = 1000$, tan $\delta = 0.05$. Integration of PZT thin films on poly-SOI substrate has been demonstrated and offers a valuable alternative to SOI substrates.

Surface Micromachining for pMEMS

Bulk micromachining means that 3-D features are etched into the bulk of crystalline and noncrystalline

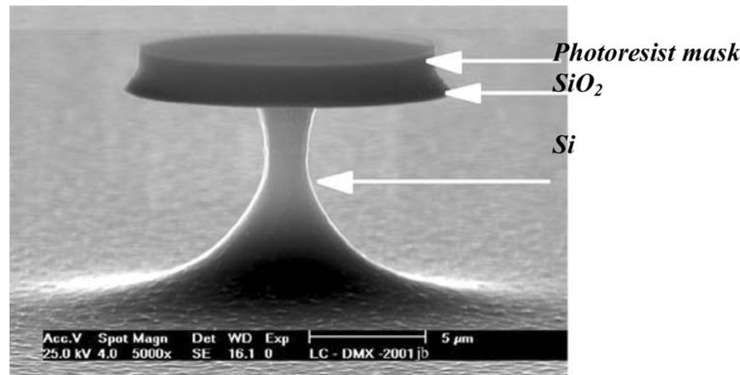


Fig. 18. SEM view of features obtained by combined anisotropic and isotropic DRIE of silicon.

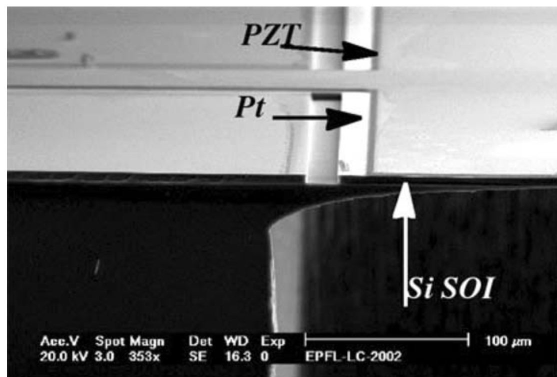


Fig. 19. SEM view of grooved membrane near the clamping point (2 μm PZT on 5 μm SOI substrate) [9].

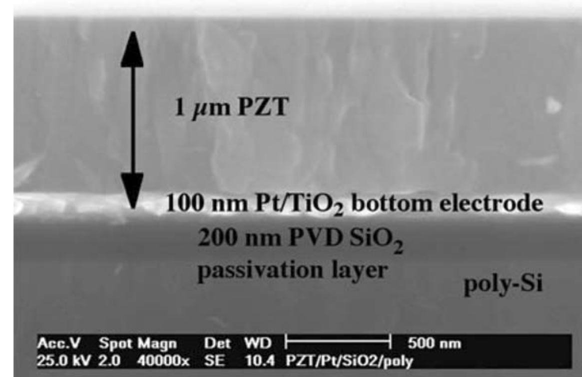


Fig. 20. SEM images cross-section of 1 μm PZT 53/47 {100}-textured thin film deposited on CMP-polished 4 μm poly-silicon layer.

materials. In contrast, surface micromachined features are built up, layer by layer, on the surface of the substrate (e.g. a single crystal silicon wafer). Dry etching defines the surface features in the x, y plane and wet etching releases them from the plane by undercutting. The overview of traditional processes, materials and developed devices can be found in literature (e.g. [5, 7] for overview).

Recently the surface micromachining has been used for fabrication of capacitive Micromachined Ultrasonic Transducers (cMUTs) [61, 62]. The feasibility of surface micromachining of Al/AlN/Pt TFBARs has been demonstrated by using PSG as sacrificial layer and Silox as removal agent [62].

However, there are still a lot of limitations concerning the compatibility of processes used for etching of the sacrificial layers with piezoelectric stack. Percin [63] has demonstrated the fabrication of piezoelectric (ZnO) ultrasonic transducer arrays by using the surface micromachining with a low temperature oxide (LTO) as sacrificial layer. An interesting alternative to wet etching methods can be the new silicon sacrificial layer dry etching (SSLDE) for free-standing RF MEMS architectures [64]. This technique uses sputtered amorphous or LPCVD polycrystalline silicon as sacrificial layers and a dry fluorine-based (SF_6) plasma chemistry as releasing process. The process is capable of various applications in surface micromachining process, and can be applied in fabricating RF MEMS switches, tunable capacitors, high-Q suspended inductors and suspended-gate MOSFETs. It has been demonstrated that the SSLDE process can release metal suspended beams and membranes with excellent performance in terms of etch rate (up to 15 μm/min), Si:SiO_2 selectivity and is fully compatible with standard

MEMS processing equipment and CMOS post-processing.

Examples of Processes of pMEMS Devices

Cantilevers Arrays

Arrays of microcantilevers (10 to 100 μm in width and 50 to 1000 μm in length) were fabricated using PZT on SOI processing (Fig. 21). Electro-mechanical properties of piezoelectric microcantilevers have been studied at the resonance in air and in vacuum (Fig. 22) and under quasistatic excitations. FEM simulations have shown excellent agreements with respect to measured resonance frequencies and coupling factor. Whatever the geometry used (test samples on thick Si or micro-cantilevers), highly reproducible $e_{31,f}$ values of -10 to -12 C/m^2 have been obtained with PZT 53/47 {100}-textured thin films [65]).

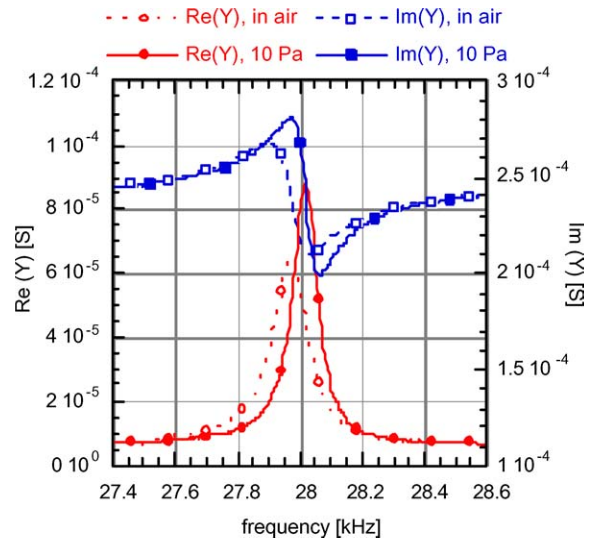


Fig. 22. Admittance curves of 1 mm × 100 μm large and 12 μm thick cantilever measured at atmospheric pressure and at 10 Pa.

Piezoelectric Ultrasonic Transducers (pMUTs)

The fabrication of piezoelectric micromachined ultrasonic transducers (pMUTs) with SOI wafers makes possible the formation of thin (2 to 50 μm) and uniform silicon diaphragm for single devices or 1D and 2D arrays. Suspended membranes down to 300 μm pitch have been fabricated to achieve resonance frequencies in the 0.5 to 1 MHz range (Figs. 23 and 24). Values of the coupling factors k^2 as high as 6% have been measured with dc bias larger than 75 kV/cm for 300 μm large membrane at 750 kHz [9].

For applications of 1D (Fig. 25(a) [9]) or 2D arrays it is crucial to have all the frequencies in a narrow range. Ideally the scattering of frequencies should not be larger than the peak width of the resonance.

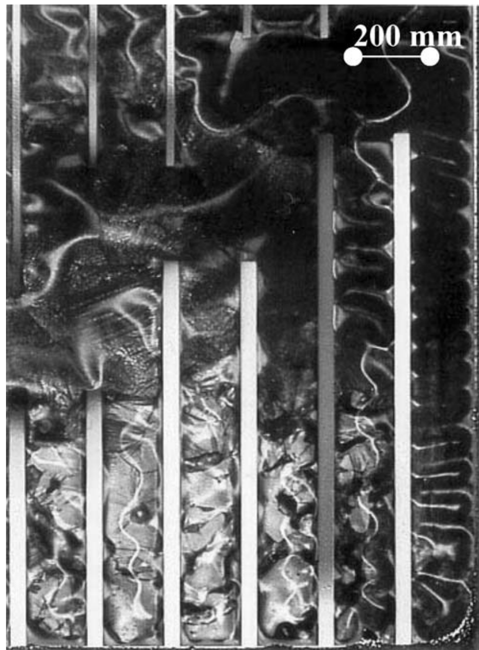


Fig. 21. Array of PZT/SOI microcantilevers. Backside view before the final release—etching of the buried SiO_2.

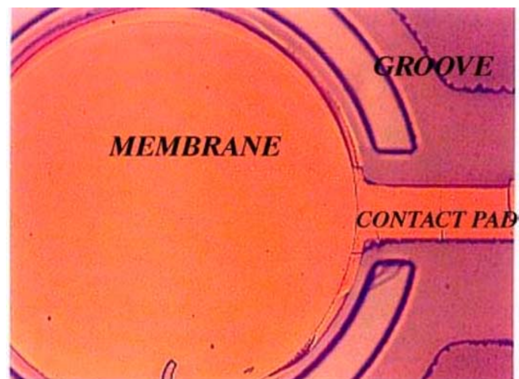


Fig. 23. Top view of 300 μm suspended membrane operating at 750 kHz [9].

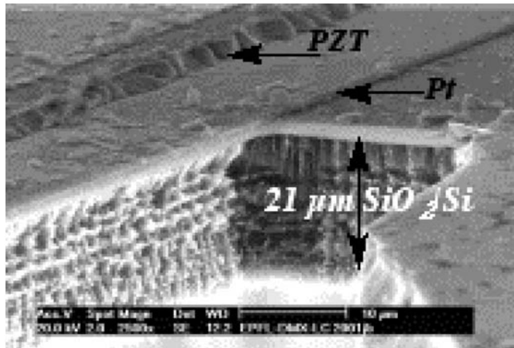


Fig. 24. SEM close-view of bridge and membrane of MUT operating at 100 kHz (2 μm PZT on 20 μm Si) [10].

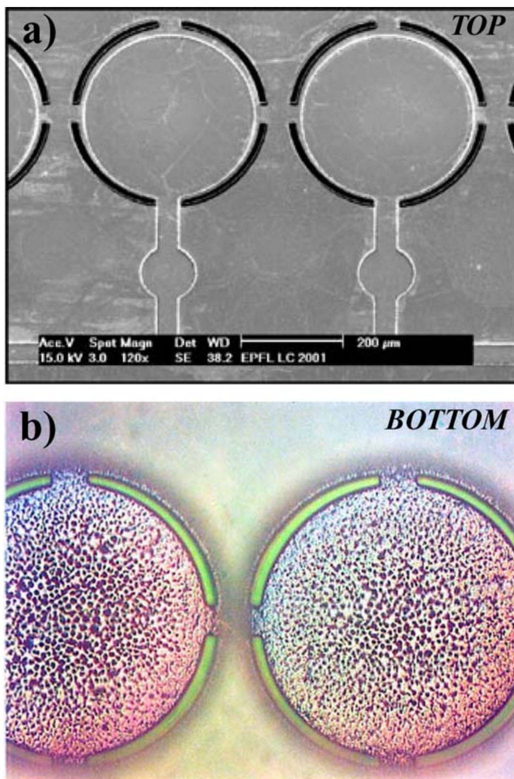


Fig. 25. Frontside and backside view of 450 micron pitch 1D array operating at 950 kHz (fully suspended membrane).

For the devices with the same geometry and boundary conditions the resonance frequency is defined by the thickness of Si membrane. Thus, the distribution of resonance frequencies is determined by the uniformity of etching of membranes (Fig. 25(b)). This was almost met with fabricated pMUT arrays. Figure 26 gives the

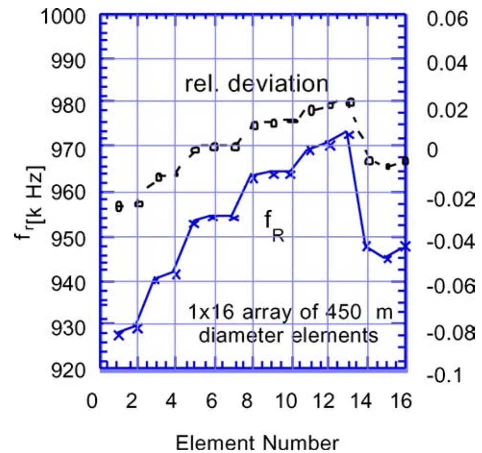


Fig. 26. Resonance frequency distribution of the 16 elements of a 1 × 16 array (450 μm diameter) measured in air.

frequency scattering within a 16 element linear array showing deviations within $+/-2.5\%$.

Pressure Sensor and Microphone

Piezoelectric cantilever and bridge acoustic sensors have been fabricated using the micromachining processes presented above. Two types of devices have been fabricated: cantilever (Fig. 27) and bridge structures. The thickness of PZT/Si membrane was 10 micron ($+/-2$ micron). To address the air leakage at low frequency, very narrow slits (3–5 μm) with very smooth and residue free sidewalls have been patterned around

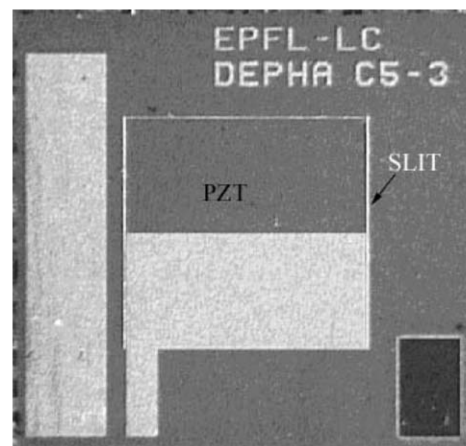


Fig. 27. Cantilever acoustic sensor, 1 micron of PZT, slit 5 μm [10].

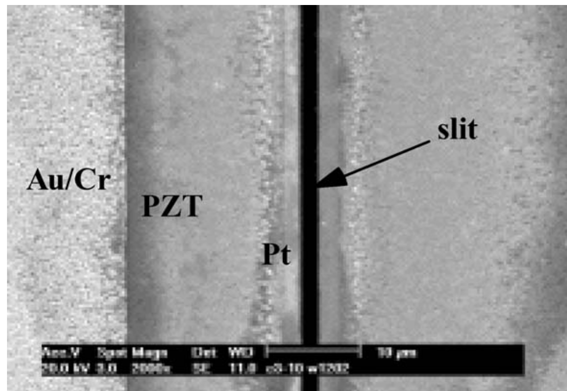


Fig. 28. SEM top view image of a 3 μm slit through PZT/Pt/SiO_2/Si. Slit width = 2 μm [9, 10].

the structures through Pt/SiO_2/Si (Fig. 28 [10]). It was thus possible to take advantage of the high sensitivity of cantilever structures to design acoustic sensors working at low frequencies (10 to 30 Hz). It has been found also that the slit conductance depends on many experimental factors such as its exact geometry, the surface roughness within of the walls or the presence of microfabrication residues. The integration of cantilever microphone into the photo-acoustic gas detector has been demonstrated. Concentration of CO_2 down to 330 ppm (air) has been detected using miniaturized photo-acoustic gas detector.

Other Devices (Non Mechanical-Devices)

FeRams. High density—low power memories, which are to be used in RF-ID cards, still represent a challenge for the semiconductor industry. The integration of ferroelectric thin films in CMOS technology represents one of the most important steps for the realization of such memories. We have investigated the complete integration of ferroelectric thin films (PZT) on W-plug in a standard 0.5 μm CMOS technology. A special process flow compatible between ferroelectrics and CMOS integrations has been designed. The most important task was to observe the impact of patterning process (plasma etching in ECR/RF RIBE) on properties of ferroelectric capacitors. Properties of PZT capacitors have been monitored after all possible process steps:

- after top electrode etching (Fig. 29(a)),
- after PZT dry etch (Fig. 29(b)),
- after IrO_2/Ir/TiN dry etch (Fig. 29(c))

In contrast to most of literature data related to patterning of ferroelectric capacitors, here no degradation of PZT ferroelectric properties at differnet steps of patterning sequencies was observed. Remanent polarization of 13 $\mu C/cm^2$ and maximum electric field of 400 kV/cm have been measured during all fabrication process and before final annealing in oxygen. This fact can be attributed to the patterning process (ECR RIBE) operating at very low working pressure (10 mPa) and using low energy ion bombardment (<25 V) in comparison to major ICP plasma reactors [66, 67].

Nanopatterning of PZT

Downscaling is an important step to achieve very high-density memories. Bühlmann et al. [68] have reported on nanopatterning of an epitaxial 200 nm thick film of $Pb(Zr_{0.40}Ti_{0.60})O_3$ (PZT) grown on conductive

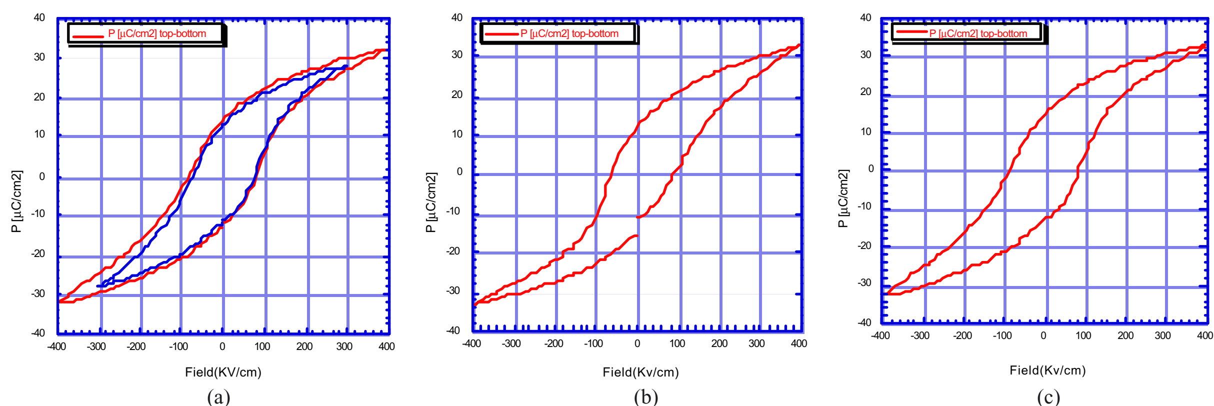


Fig. 29. Ferroelectric loops measured on Pt/PZT/IrO_2/Ir stack: (a) after Pt top electrode etching, (b) after PZT dry etching, (c) after IrO_2/Ir/TiN dry etching.

Nb-doped $SrTiO_3$ (100). Patterning of PZT has been done by e-beam lithography using PMMA (polymethylmethacrylate) resist, Cr as hard and sacrificial mask and ECR/RF RIBE etching. For lithography, a 150 nm thick PMMA film was deposited. Patterns with lateral dimension between 50 and 200 nm were written by an e-beam. After the development, noncontact atomic force microscopy scans on the PMMA showed that holes down to 50 nm were obtained. A 75 nm thin Cr masking layer was evaporated onto the developed PMMA and the lift off was performed in acetone. Scanning electron microscopy observations on the Cr patterns showed that the patterning worked for all features with lateral dimensions larger than 50 nm. The PZT film and Cr sacrificial mask were then etched in a dual frequency ECR/RF reactor using a $CF_4/CCl_4/Ar$ gas mixture at a low pressure of 10 mPa. This process assures a good balance between chemical and physical etching. Ion energies have been kept small. A small rf self-bias of only 25 V was applied to the substrate. The ions leaving the ECR ion gun had energies in the range of 200 to 300 eV at maximum. The etching rate was found to be 10 nm/min for PZT and 3 nm/min for Cr. The remaining Cr was removed in an aqueous solution of ceric ammonium nitrate and perchloric acid. In contrast to Ar ion milling [69], this etching process did not leave any redeposited PZT. The dry etching process lead to rounded PZT patterns caused by a continuous reduction of the thinner border of the Cr-mask patterns (Fig. 30). The smallest items achieved had a lateral dimension of 100 nm. Piezoelectric sensitive scanning force microscopy in the contact mode revealed a strong increase of the piezoelectric response for feature sizes with lateral dimensions below 200 nm.

Local Growth and Crystallization of Piezoelectric Films [70]

Piezoelectric and pyroelectric films of perovskite materials need high processing temperatures of more than 600°C. This may damage the rest of the device and is especially critical for monolithic integration together with the read-out or driving circuit. In our studies, PZT ($PbZr_xTi_{1-x}O_3$) thin films have been locally grown by means of sol-gel deposition and local anneals on microhotplate integrated in the substrate. The microhotplate was based on a tantalum silicide filament (Ta_5Si_3 [71]) formed on stress compensated SiN/SiO_2 membrane. On this filament, a passivation layer of SiO_2, a layer of Ti/TiO_2 and a bottom electrode of Pt were deposited by sputtering. After the deposition of PZT sol-gel solution, the film is pyrolized and crystallized by applying the electrical power to the hot-plate (Fig. 31). Due to the low heat conductivity of the membrane, crystallization of the PZT film occurs exactly ($+/-1\ \mu$m) on the resistor filament. The formation of crystalline, i.e. perovskite PZT was verified by means of X-ray diffraction (Fig. 32). A random PZT texture has been observed.

Microfabrication of pMEMS—Final Remarks

In this paper, critical issues for microfabrication of piezoelectric MEMS have been discussed. To overcome resolution problems in complex device

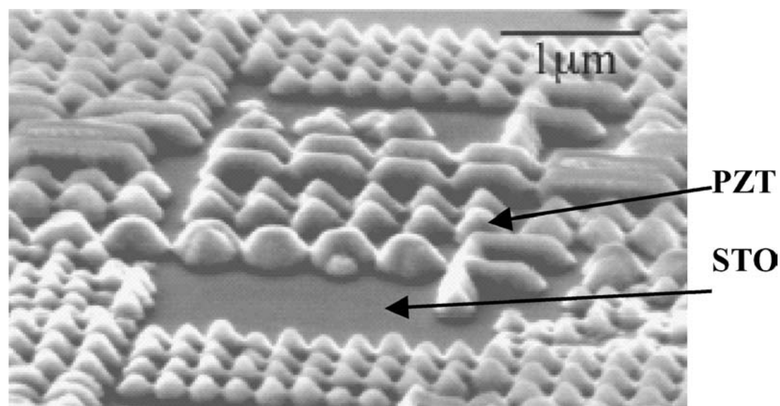


Fig. 30. SEM view of nanopatterned PZT features on STO [68].

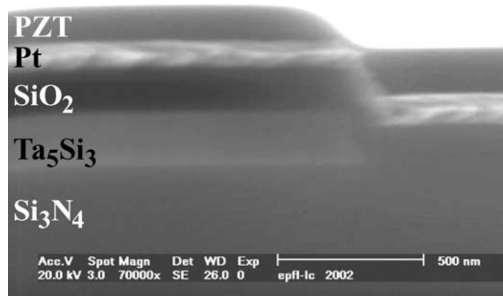


Fig. 31. SEM cross section view of pyrolized PZT grown locally on TaSi microhotplate [70].

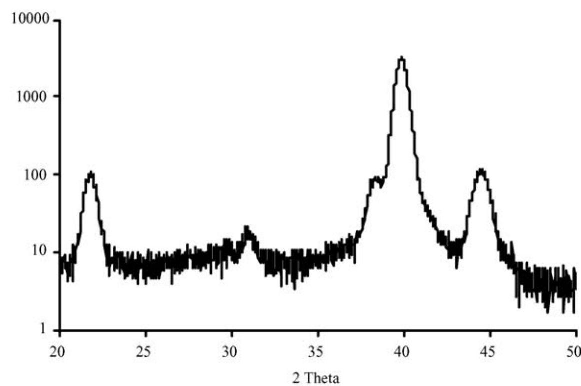


Fig. 32. XRD spectra showing the (100), (110), (111) and (200) orientation of PZT grown on the membrane.

structures, wet etching of PZT films and platinum bottom electrodes have been replaced by high density plasma dry etching methods. Micron scale patterns have been obtained using reactive ion beam etching (ECR/RF RIBE) processes. Due to working pressures two order of magnitude lower than in conventional reactive ion etching (RIE/ICP) reactors (10 mPa compared to 1 Pa), RIBE processes were found to be much less sensitive to redeposition of etching by-products. The developed processes exhibited also much higher etching rates and better results in term of anisotropy, photoresist stability and removability. These new processes have been successfully integrated into a microfabrication sequence that fully preserves the functionality of piezoelectric thin films. At the end of the micromachining sequence, transverse piezoelectric coefficient $e_{31,f}$ of -12 C/m^2, dielectric permittivity ε of 1100 and loss factor tan δ of 0.03 (at 1 kHz) have been measured on test samples with 1 μm PZT 53/47 {100}-textured thin film.

In-plane laminated PZT/Si structures have been obtained by compensating the tensile stress of platinum bottom electrode and PZT film with compressive SiO_2 thermal oxide. In PZT films, the increase of stress due to poling (up to 50%) has to be considered as well. Finally, the integration of PZT thin films on SOI or thick polysilicon layer has been demonstrated.

Several examples of piezoelectric devices presented in this paper have been developed during the last years. It has been demonstrated that the microfabrication of piezoelectric MEMS based on thin film PZT is the versatile and reliable technology.

References

1. P. Muralt, *J. Micromech. Microeng.*, **10**, 136 (2000).
2. N. Setter (Ed.), *Piezoelectric Materials and Devices*, Lausanne (2002).
3. Y. Miyahara, *Appl. Surf. Sci.*, **140**, 428 (1999).
4. P. Muralt, *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, **47**(4), 903 (2000).
5. M. Elwenspoek and H. Jansen, *Silicon Micromachining* (C.U. Press, Cambridge, 1998).
6. W. Lang, *Materials Science and Engineering*, **R17**, 1 (1996).
7. M. Madou, *Fundamentals of Microfabrication* (CRC Press, Boca Raton, 1997).
8. S.J. Gross et al., *Proceedings of the SPIE*, **4558**, 72 (2001).
9. J. Baborowski, N. Ledermann, S. Gentil, and P. Muralt, *The 11th International Conference on Solid-State Sensors and Actuators* (Munich, Germany, June 10–14, 2001), p. 596.
10. P. Muralt et al., in *Materials and Process Integration for MEMS*, edited by P.F.E.H. Tay (Kluwer Academic Publishers, The Netherlands, 2002), p. 3.
11. D.R. Lide (Ed.), *Handbook of Chemistry and Physics* (CRC Press, 1995).
12. D.L. DeVoe and A.P. Pisano. *Transducers '97, International Conference on Solid-State Sensors and Actuators* (Chicago, 1997).
13. J.H. Kim et al., *Integrated Ferroelectrics*, **15**, 325 (1997).
14. A.M. Flynn et al., *J. Microelectromechanical Sytems*, **1**, 44 (1992).
15. M.-A. Dubois and P. Muralt, *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, **45**(5), 1169 (1998).
16. G.-A. Racine, P. Muralt, and M.-A. Dubois, *Smart Mater. Struct.*, **7**, 404 (1998).
17. J. Baborowski et al., *Ferroelectrics*, **224**, 283 (1999).
18. K. Kunz, P. Enoksson, and G. Stemme, *Sensors and Actuators A*, **92**, 156 (2001).
19. S.S. Lee and R.M. White, *J. Micromech. Microeng.*, **8**, 230 (1998).
20. A. Schroth et al., *Sensors and Actuators A*, **73**, 144 (1999).
21. C. Lee, T. Itoh, and T. Suga, *Sensors and Actuators A*, **72**, 179 (1999).
22. J.J. Bernstein et al., *IEEE Tran. UFFC*, **44**(5), 960 (1997).
23. J. Baborowski, N. Ledermann, and P. Muralt, *Proceedings of IEEE Ultrasonic Symposium* (Münich, Germany, 2002).

24. T. Maeder, L. Sagalowicz, and P. Muralt, *Jpn. J. Appl. Phys.*, **37**, 2007 (1998).
25. P. Muralt et al., *J. Appl. Phys.*, **83**(7), 3835 (1998).
26. T. Maeder et al., *British Ceram. Proc.*, **54**, 206 (1995).
27. B. Kloeck et al., *IEEE Transactions on Electron Devices*, **36**(4), 663 (1989).
28. P. Fluckiger et al., Standard processes at the Center of Microtechnology–EPFL, 2002, http://microtechnique.epfl.ch/cmi/.
29. J. Hopwood, *Plasma Sources Science and Technology*, **1**, 109.
30. J. Baborowski, P. Muralt, and N. Ledermann, *Integrated Ferroelectrics*, **27**, 243 (1999).
31. J. Baborowski et al., *Vacuum*, **56**, 51 (2000).
32. M. Sugawara, *Plasma Etching Fundamentals and Applications* (Oxford Science Publications, 1998).
33. S. Marks , L.G. Jerde, G. Celii, S.A. Aggarwal, and J.S. Martin, *Proceedings of ISAF* (Nara, 2002).
34. http://www.tegal.com/news_events/nr/nr020718.html
35. E. Lee et al., *Integrated Ferroelectrics*, **16**, 165 (1997).
36. S. Troiler-McKinstry et al. *International Symposium of Applied Ferroelectrics* (ISAF, Bethlehem, 1986).
37. H. Macé, H. Achard, and L. Peccoud, *Microelectronic Engineering* **29**, 45 (1995).
38. R. Zeto et al., *Mat. Res. Soc. Symp. Proc.*, **546**, 159 (1999).
39. W. Pan et al., *J. Mater. Res.*, **9**(11), 2976 (1994).
40. C.W. Chung, *J. Vac. Sci. Technol. B*, **16**(4), 1894 (1998).
41. J.-K. Jung and W.-J. Lee, *Jpn. J. Appl. Phys.*, **40**, 1408 (2001).
42. Chee Won Chung, Yo Han Byun, and Hye In Kim, *Microelectronic Engineering*, **63**, 353 (2002).
43. K. Williams et al. *IEEE International Symposium on Application of Ferroelectrics (ISAF'96)* (1996).
44. F. Boukari et al., *Rev. Sci. Instrum.*, **65**(4), 1097 (1994).
45. J. Baborowski et al., *Integrated Ferroelectrics*, **31**, 261 (2000).
46. J.L. Vossen and W. Kern, *Thin Film Process*, 1st ed. Vol. V-1. (Academic Press, New-York, 1978).
47. R.P. Frankenthal and D.H. Eaton, *J. Electrochem. Soc.*, **123**(5), 703 (1976).
48. C. Farrell, K. Milkove, C. Wang, and D. Kotecki, *Integrated Ferroelectrics*, **16**, 109 (1997).
49. K.L. Milkove, J.A. Coffin, and C. Dziobkowski, *J. Vac. Sci. Technol.* **A16**(3), 1483 (1998).
50. Celli et al., *Integrated Ferroelectrics*, **27**, 227 (1999).
51. T. Sakoda et al., *Japanese Journ. Appl. Phys. pI*, **40**, 2911 (2001).
52. Chung et al., *Integrated Ferroelectrics*, **39**, 119 (2001).
53. Chung et al., *Journal of Vac. Sc & Technol. A*, **19**, 2400 (2001).
54. Chongying Xu et al., *Ferroelectric Thin Films VII*, MRS, 129 (1999).
55. M.C. Chianga et al., *Electrochemical Society Proceedings*, **99**, 114 (2000).
56. Eunk-Jik Lee, Jin-Woong Kim, and Won-Jong Lee, *Jpn. J. Appl. Phys.*, **37**, 2634 (1998).
57. Wei Pan and S.B. Desu, *Phys. Stat. Sol., (a)* **161**, 201 (1997).
58. F. Lärmer and A. Schilp, Patent US6284148: Method for anisotropic etching of silicon, USA, 2001.
59. A.M. Hynes et al., *Sensors and Actuators A*, **74**, 13 (1999).
60. A.A. Yasseen, N.J. Mourlas and M. Mehregany, *J. Electrochem. Soc.*, **144**(1), 237 (1997).
61. X.J. Ladabaum and B.T. Khuri-Yakub, *Ultrasonic*, **36**, 25 (1998).
62. E. Cianci, V. Foglietti, G. Caliano, and M. Pappalardo, *Microelectronic Engineering*, **61/62**, 1025 (2002).
63. G. Percin and B.T. Khuri-Yakub, *Ultrasonics*, **40** 441 (2002).
64. S. Frédérico, C. Hibert, R. Fritschi, Ph. Flückiger, Ph. Renaud, and A.M. Ionescu, *Proceedings of the 16th IEEE International Conference on Micro Electro Mechanical Systems (MEMS '03)* (Kyoto, Japan, 2003), p. 570.
65. N. Ledermann, P. Muralt, J. Baborowski, S. Gentil, K. Mukati, M. Cantoni, A. Seifert, and N. Setter, *Sensors and Actuators A*, **105**, 162 (2003).
66. M.-G. Kang, K.-T. Kim, and C.-I. Kim, *Thin Solid Films*, **398/399**, 448 (2001).
67. M.-G. Kang, K.-T. Kim, and C.-I. Kim, *Thin Solid Films*, **435**, 222 (2003).
68. S. Bühlmann, B. Dwir, J. Baborowski, and P. Muralt, *Applied Physics Letters*, **80**(17), 3195 (2002).
69. M. Hiratani, C. Okazaki, H. Hasegawa, N. Sugii, Y. Tarutani, and K.Takagi, *Jpn. J. Appl. Phys.*, Part 1, **36**, 5219 (1997).
70. F. Calame, J. Baborowski, N. Ledermann, P. Muralt, S. Gentil, and N. Setter, *Integrated Ferroelectrics*, **54**, 549 (2003).
71. A. Pollien, N. Ledermann, J. Baborowski, and P. Muralt, Patent, WO 02/080620, 10.10.2002.